DW-CAOC12-1XXC
CXP-CXP Active Optical Cable

Features

♦ Full duplex 12 channels 850nm parallel active optical cable

♦ Transmission data rate up to 10.3Gb/s per channel

♦ Hot pluggable electrical interface

♦ Differential AC-coupled high speed data interface

♦ 12 channels 850nm VCSEL array

♦ 12 channels PIN photo detector array

♦ Multi-mode optical fibre cable of up to 300m(OM3) or 400m(OM4)

♦ Low power consumption < 2W

♦ Operating case temperature 0°C to +70°C

♦ 3.3V power supply voltage

♦ RoHS 6 compliant

Applications

♦ Infiniband transmission at 12ch SDR, DDR and QDR

♦ Switches, Routers

♦ Data Centers

♦ Other 120G Interconnect Requirement

Description

CXP-CXP active optic cables are a high performance, low power consumption, long reach interconnect solution supporting 120G Ethernet, fiber channel and PCIe. It is compliant with the 120Gbits Small Form factor Hot-Pluggable CXP-interface. DONGWE CXP AOC is an assembly of 12 full-duplex lanes, where each lane is capable of transmitting data at rates up to 10Gb/s, providing an aggregated rate of 120Gb/s.
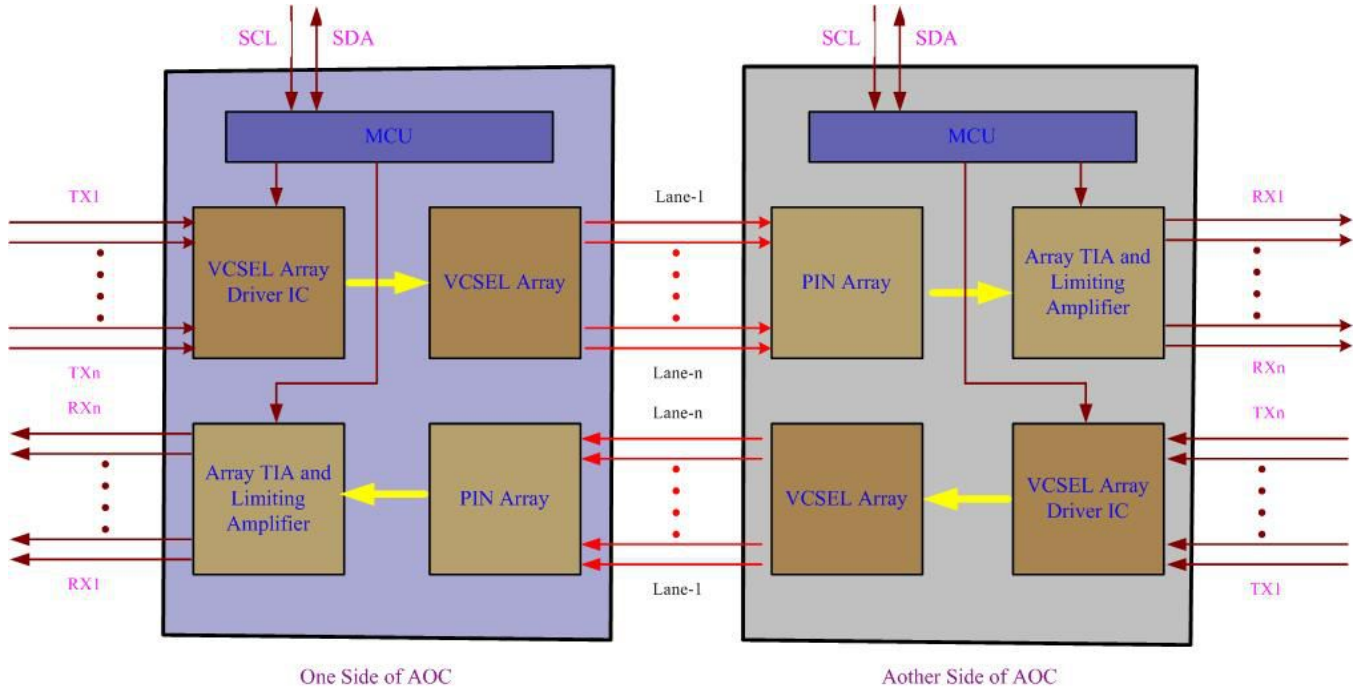
Figure1. Module Block Diagram

AOC is one kind of parallel transceiver. VCSEL and PIN array package is key technique, through I2C system can contact with module.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-20	85	℃
Case Operating Temperature	Top	0	70	℃
Humidity(non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case temperature	Tca	0		70	ºC
Data Rate Per Lane	fd	2.5		10.3	Gbps
Humidity	Rh	5		85	%
Power Dissipation	Pm			2	W
Fiber Bend Radius	Rb	3			cm

Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential input impedance	Zin	90	100	110	ohm
Differential Output impedance	Zout	90	100	110	ohm
Differential input voltage amplitude aAmplitude	ΔVin	200		1200	mVp-p
Differential output voltage amplitude	ΔVout	600		800	mVp-p
Skew	Sw			300	ps
Bit Error Rate	BR			E-12	
Input Logic Level High	VIH	2.0		VCC	V
Input Logic Level Low	VIL	0		0.8	V
Output Logic Level High	VOH	VCC-0.5		VCC	V
Output Logic Level Low	VOL	0		0.4	V

Note：
1. BER=10^-12; PRBS 2^31-1@10.3125Gbps.
2. Differential input voltage amplitude is measured between TxnP and TxnN
3. Differential output voltage amplitude is measured between RxnP and RxnN

Pin Descriptions

Pin	Logic	Symbol	Name/Description	Ref.
A1		GND	Module Ground	1
A2	CML-I	Tx1+	Transmitter non-inverted data input	
A3	CML-I	Tx1-	Transmitter inverted data input	
A4		GND	Module Ground	1
A5	CML-I	Tx3+	Transmitter non-inverted data input	
A6	CML-I	Tx3-	Transmitter inverted data input	
A7		GND	Module Ground	1
A8	CML-I	Tx5+	Transmitter non-inverted data input	
A9	CML-I	Tx5-	Transmitter inverted data input	
A10		GND	Module Ground	1
A11	CML-I	Tx7+	Transmitter non-inverted data input	
A12	CML-I	Tx7-	Transmitter inverted data input	
A13		GND	Module Ground	1
A14	CML-I	Tx9+	Transmitter non-inverted data input	
A15	CML-I	Tx9-	Transmitter inverted data input	
A16		GND	Module Ground	1
A17	CML-I	Tx11+	Transmitter non-inverted data input	
A18	CML-I	Tx11-	Transmitter inverted data input	
A19		GND	Module Ground	1
A20	LVCMOS-I	SCL	2-wire Serial interface clock	2
A21	LVCMOS-I/O	SDA	2-wire Serial interface data	2
B1		GND	Module Ground	1
B2	CML-I	Tx0+	Transmitter non-inverted data input	
B3	CML-I	Tx0-	Transmitter inverted data input	
B4		GND	Module Ground	1
B5	CML-I	Tx2+	Transmitter non-inverted data input	
B6	CML-I	Tx2-	Transmitter inverted data input	
B7		GND	Module Ground	1
B8	CML-I	Tx4+	Transmitter non-inverted data input	
B9	CML-I	Tx4-	Transmitter inverted data input	
B10		GND	Module Ground	1
B11	CML-I	Tx6+	Transmitter non-inverted data input	
B12	CML-I	Tx6-	Transmitter inverted data input	

B13		GND	Module Ground	1
B14	CML-I	Tx8+	Transmitter non-inverted data input	
B15	CML-I	Tx8-	Transmitter inverted data input	
B16		GND	Module Ground	1
B17	CML-I	Tx10+	Transmitter non-inverted data input	1
B18	CML-I	Tx10-	Transmitter inverted data input	
B19		GND	Module Ground	1
B20		VCC3.3-TX	+3.3v Transmitter Power Supply	
B21		VCC12-TX	+12v Transmitter Power Supply, Unconnected	
C1		GND	Module Ground	1
C2	CML-O	RX1+	Receiver non-inverted data output	
C3	CML-O	RX1-	Receiver inverted data output	
C4		GND	Module Ground	1
C5	CML-O	RX3+	Receiver non-inverted data output	
C6	CML-O	RX3-	Receiver inverted data output	
C7		GND	Module Ground	1
C8	CML-O	RX5+	Receiver non-inverted data output	
C9	CML-O	RX5-	Receiver inverted data output	
C10		GND	Module Ground	1
C11	CML-O	RX7+	Receiver non-inverted data output	
C12	CML-O	RX7-	Receiver inverted data output	
C13		GND	Module Ground	1
C14	CML-O	RX9+	Receiver non-inverted data output	
C15	CML-O	RX9-	Receiver inverted data output	
C16		GND	Module Ground	1
C17	CML-O	RX11+	Receiver non-inverted data output	
C18	CML-O	RX11-	Receiver inverted data output	
C19		GND	Module Ground	1
C20	LVTTL-O	PRSNT_L	Module Present, pulled down to GND	
C21	LVTTL-I/O	INT_L/Reset_L	Interrupt output, Module Reset	2
D1		GND	Module Ground	1
D2	CML-O	RX0+	Receiver non-inverted data output	
D3	CML-O	RX0-	Receiver inverted data output	
D4		GND	Module Ground	1
D5	CML-O	RX2+	Receiver non-inverted data output	

D6	CML-O	RX2-	Receiver inverted data output	
D7		GND	Module Ground	1
D8	CML-O	RX4+	Receiver non-inverted data output	
D9	CML-O	RX4-	Receiver inverted data output	
D10		GND	Module Ground	1
D11	CML-O	RX6+	Receiver non-inverted data output	
D12	CML-O	RX6-	Receiver inverted data output	
D13		GND	Module Ground	1
D14	CML-O	RX8+	Receiver non-inverted data output	
D15	CML-O	RX8-	Receiver inverted data output	
D16		GND	Module Ground	1
D17	CML-O	RX10+	Receiver non-inverted data output	
D18	CML-O	RX10-	Receiver inverted data output	
D19		GND	Module Ground	1
D20		VCC3.3-RX	+3.3v Receiver Power Supply	
D21		VCC12-RX	+12v Receiver Power Supply, Unconnected	

Notes:
1. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector; should be pulled up with 4.7k – 10k ohms on host board to a voltage between 3.15Vand 3.6V.

Receiver -- Top Card

C1	GND				GND	D1
C2		Rx1p		Rx0p		D2
C3		Rx1n		Rx0n		D3
C4	GND				GND	D4
C5		Rx3p		Rx2p		D5
C6		Rx3n		Rx2n		D6
C7	GND				GND	D7
C8		Rx5p		Rx4p		D8
C9		Rx5n		Rx4n		D9
C10	GND				GND	D10
C11		Rx7p		Rx6p		D11
C12		Rx7n		Rx6n		D12
C13	GND				GND	D13
C14		Rx9p		Rx8p		D14
C15		Rx9n		Rx8n		D15
C16	GND				GND	D16
C17		Rx11p		Rx10p		D17
C18		Rx11n		Rx10n		D18
C19	GND				GND	D19
C20		PRSNT_L		Vcc3.3-Rx		D20
C21		Int_L/Reset_L		Vcc12-Rx		D21

Card Edge

Transmitter -- Bottom Card

A1	GND						GND	B1
A2		Tx1p				Tx0p		B2
A3		Tx1n				Tx0n		B3
A4	GND						GND	B4
A5		Tx3p				Tx2p		B5
A6		Tx3n				Tx2n		B6
A7	GND						GND	B7
A8		Tx5p				Tx4p		B8
A9		Tx5n				Tx4n		B9
A10	GND						GND	B10
A11		Tx7p				Tx6p		B11
A12		Tx7n				Tx6n		B12
A13	GND						GND	B13
A14		Tx9p				Tx8p		B14
A15		Tx9n				Tx8n		B15
A16	GND						GND	B16
A17		Tx11p				Tx10p		B17
A18		Tx11n				Tx10n		B18
A19	GND						GND	B19
A20		SCL				Vcc3.3-Tx		B20
A21		SDA				Vcc12-Tx		B21

(Card Edge)

Figure2. Electrical Pin-out Details

PRSNT_L Pin：

PRSNT_L is used to indicate when the module is plugged into the host receptacle. It is pulled down to GND through 5.2 kOhm in modules requiring 12V power, and tied directly down to GND in modules requiring 3.3V power only. DONGWE CXP Prsnt_L Pin internal directly connected to GND and just need single +3.3V Power Supply. The PRSNT_L signal is asserted "Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

Int_L/Reset_L Pin：

Int_L/Reset_L is a bidirectional signal. When driven from the host, it operates logically as a Reset signal. When driven from the module, it operates logically as an Interrupt signal. In both cases, the signal is asserted low, as indicated by the '_L' suffix. The Int_L/Reset_L signal requires open collector outputs in both the host and module, and must be pulled up on the host board. Int_L and Reset_L indications are distinguished from each other by timing - a shorter assertion, driven by the module, indicates an interrupt, and a longer assertion of the signal, driven by the host, indicates a reset.

Int_L operation:

When Int_L/Reset_L is pulled "Low" by the module for longer than the minimum interrupt pulse width (tInt_L,PW-min) and shorter than the maximum interrupt pulse width (tInt_L,PW-max) the signal signifies an interrupt. An interrupt indicates a possible module operational fault or a module status critical to the host system. The host identifies the cause of the interrupt using the 2-wire serial interface. Int_L must operate in pulse mode (vs. static mode), in order to distinguish a short interrupt signal from a longer

reset signal, so the module must de-assert Int_L/Reset_L after the interrupt has been signaled.

Power Supply Filtering

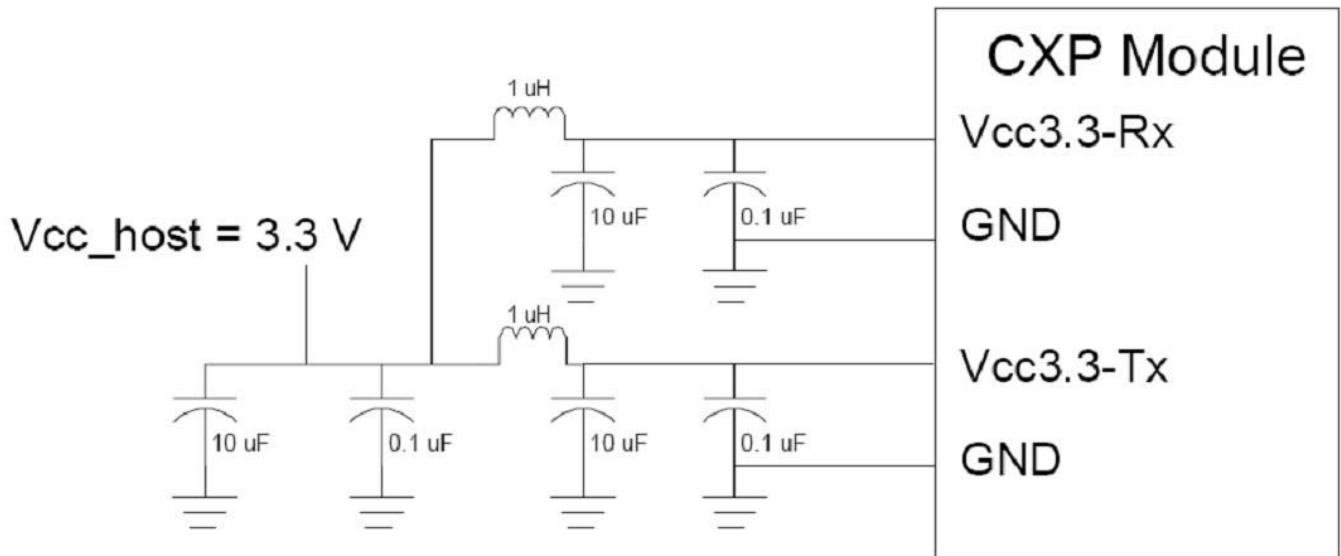The host board should use the power supply filtering shown in Figure3.

Figure3. Host Board Power Supply Filtering

Timing for Soft Control and Status Functions

Parameter	Symbol	Max	Unit	Conditions
Initialization Time	t_init	2000	ms	Time from power on[1], hot plug or rising edge of Reset until the module is fully functional[2]
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on[1] until module responds to data transmission over the 2-wire serial bus
Monitor Data Ready Time	t_data	2000	ms	Time from power on[1] to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
Reset Assert Time	t_reset	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional[2]
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL = Vol

Parameter	Symbol		Unit	Conditions
IntL Deassert Time	toff_IntL	500	µs	Time from clear on read[3] operation of associated flag until Vout:IntL = Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Interrupt Pulse Max Width	tintL,PW-max	50	µs	Max Time from falling edge of int_L pin output to rising edge of int_L pin output
Rx LOS Assert Time	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set and IntL asserted
Tx Fault Assert Time	ton_Txfault	200	ms	Time from Tx Fault state to Tx Fault bit set and IntL asserted
Flag Assert Time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted
Mask Assert Time	ton_mask	100	ms	Time from mask bit set[4] until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask	100	ms	Time from mask bit cleared[4] until associated IntlL operation resumes
Power_over-ride or Power-set Assert Time	ton_Pdown	100	ms	Time from P_Down bit set [4] until module power consumption enters lower Power Level
Power_over-ride or Power-set Deassert Time	toff_Pdown	300	ms	Time from P_Down bit cleared[4] until the module is fully functional3
Parameter	**Symbol**	**Min**	**Unit**	**Conditions**
Interrupt Pulse Min Width	tintL,PW-min	5	µs	Min Time from falling edge of int_L pin output to rising edge of int_L pin output
Reset Pulse Min Width	Trst,PW-min	25	ms	Min Time from falling edge of Reset pin input to rising edge of Reset pin input

Note：
1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum specified value.
2. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 deasserted.
3. Measured from falling clock edge after stop bit of read transaction.
4. Measured from falling clock edge after stop bit of write transaction.

Figure5. Timing Specifications
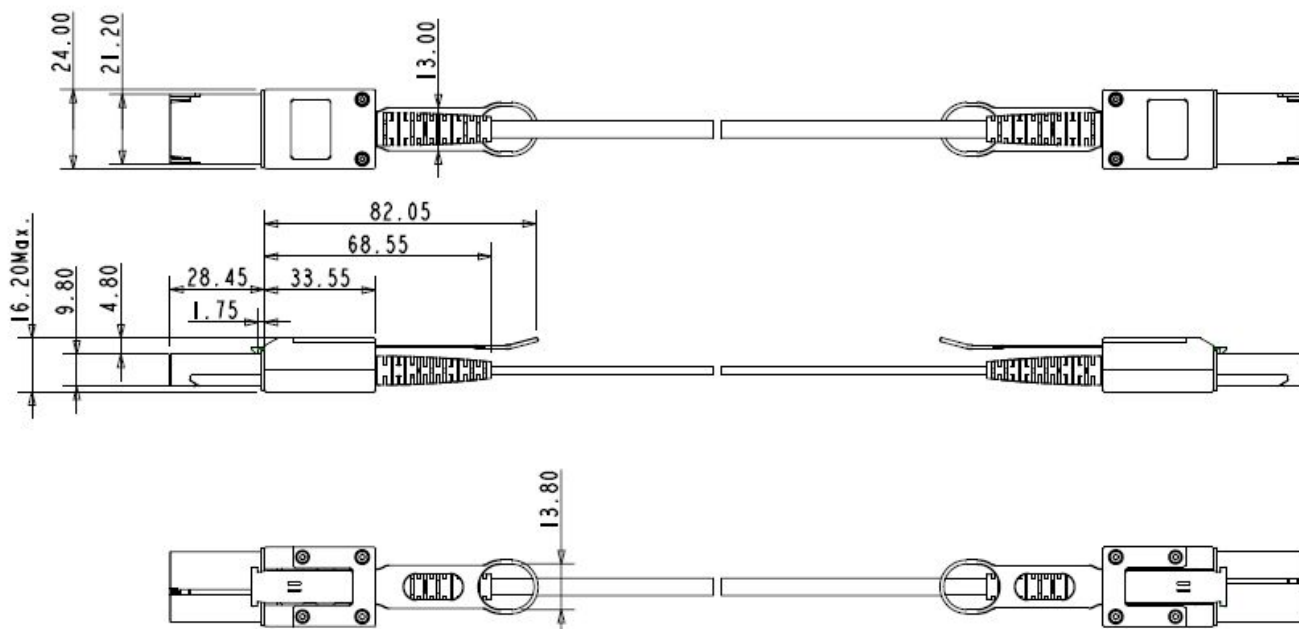
Mechanical Dimensions

Figure6. Mechanical Specifications

Ordering information

Part Number	Product Description
DW-CAOC12-1003C	CXP Active Optical Cable, 120G,3m
DW-CAOC12-1005C	CXP Active Optical Cable, 120G,5m
DW-CAOC12-1050C	CXP Active Optical Cable, 120G,50m
DW-CAOC12-1XXXC	CXP Active Optical Cable, 120G,XXXm (XXX from 1 to 300)

XX	Cable Length
03	03=3m
05	05=5m
10	10=10m
20	20=20m
50	50=50m
X1	X1=100m
X2	X3=300m

References

120Gbit/s Small Form-factor Hot-Pluggable CXP-interface

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